WHAT IS CLAIMED IS:

1. A method for forming a trench DMOS, comprising the steps of:

providing an article comprising a substrate of a first conductivity type and a body region of a second conductivity type, said article having a trench which extends through said body region and said substrate;

depositing a gate oxide layer in the trench;

forming a gate in the trench, said gate having at least one layer comprising a material selected from the group consisting of polycide and refractory metals; and

forming a source region in the body region;

wherein the source region is formed after the gate oxide layer is deposited.

2. The method of claim 1, wherein said gate comprises a first layer comprising undoped polysilicon, a second layer comprising doped polysilicon, and a third layer comprising a material selected from the group consisting of polycide and refractory metals.

3. The method of claim 2, wherein said first layer is adjacent to said gate oxide layer.

4. The method of claim 1, wherein said gate has at least one layer comprising a refractory metal.

5. The method of claim 4, wherein said refractory metal is selected from the group consisting of W and TiW.

6. The method of claim 1, wherein said gate has at least one layer comprising polycide.

7. The method of claim 6, wherein said polycide is selected from the group consisting of WSi_2 and $TiSi_2$.

8. The method of claim 1, wherein said trench is formed by providing a masking layer defining at least one trench, and forming the trench defined by the masking layer.

9. The method of claim 8, wherein said masking layer is disposed on said body region before said trench is formed.

10. The method of claim 8, wherein said mask is removed after said trench is formed.

11. The method of claim 1, wherein said body region is a P-body.

12. The method of claim 1, wherein said body region is formed by implanting and diffusing a dopant into the substrate.

13. The method of claim 1, wherein the body region is disposed on said substrate.

14. The method of claim 1, wherein the source region is a source region of said first conductivity type.

15. The method of claim 14, further comprising the step of forming a source region of a third conductivity type.

16. The method of claim 15, wherein the first conductivity type is n+ and the third conductivity type is p+.

17. The method of claim 1, wherein said source region is an n+ source region.

18. The method of claim 1, wherein said source region is adjacent to said trench.

19. The method of claim 1, wherein said source region is formed with a junction depth of less than about 0.5 μm.

20. The method of claim 1, wherein said source region is formed with a junction depth within the range of about 0.2 to about 0.5 μm.

21. The method of claim 1, further comprising the step of:
forming a patterned BPSG layer over said trench.

22. The method of claim 21, wherein the patterned BPSG layer is formed over the trench with a flow temperature cycle ranging from about 900 to about 950°C.

23. A trench DMOS made in accordance with the method of claim 19, said trench DMOS comprising a plurality of gate electrodes, and wherein each of said gate electrodes has a BPSG region associated with it.

24. A trench DMOS made in accordance with the method of claim 1.

25. The trench DMOS of claim 24, further comprising a drain, wherein the distance between at least a portion of said gate and said drain is greater than the distance between said source region and said drain.

26. The method of claim 1, wherein the step of forming a gate in the trench includes the steps of filling the trench with polysilicon, and depositing on the polysilicon a layer comprising a material selected from the group consisting of polycide and refractory metals.

27. A method for making a trench DMOS, comprising the steps of:

providing a substrate of a first conductivity type;

forming a body region on the substrate, said body region having a second conductivity type;

forming a masking layer defining at least one trench;

forming the trench defined by the masking layer, said trench extending through the body region and the substrate;

forming a gate in the trench, said gate comprising a first layer comprising undoped polysilicon, a second layer comprising doped polysilicon, and a third layer comprising a material selected from the group consisting of polycide and refractory metals; and

forming a first source region of the first conductivity type in the body region adjacent to the trench.

28. The method of claim 27, further comprising the step of:

forming a second source region of a third conductivity type adjacent to said first source region.

29. The method of claim 28, wherein said first source region is an n+ source, and wherein said second source region is a p+ source.

30. The method of claim 27, wherein said trench is covered with an insulating layer before said gate is formed.

31. The method of claim 30, wherein said insulating layer is a gate oxide layer.

32. A trench DMOS, comprising:

a substrate having a first conductivity type;

a body region having a second conductivity type;

a trench which extends through said body region and said substrate;

a gate, disposed in said trench;

a source region disposed in said body region; and

a drain;

wherein the distance between at least a portion of said gate and said drain is greater than the distance between said source region and said drain.

33. The trench DMOS of claim 32, wherein said substrate has a major surface which is substantially planar, and wherein the axis is perpendicular to said major surface.

34. The trench DMOS of claim 32, further comprising a gate oxide layer disposed between said gate and the surface of said trench.

35. The trench DMOS of claim 32, wherein said gate comprises a first layer comprising undoped polysilicon, a second layer comprising doped polysilicon, and a third layer comprising a material selected from the group consisting of polycide and refractory metals.

36. The trench DMOS of claim 35, wherein said first layer is adjacent to said gate oxide layer.

37. The trench DMOS of claim 32, wherein said gate has at least one layer comprising a refractory metal.

38. The trench DMOS of claim 37, wherein said refractory metal is selected from the group consisting of W and TiW.

39. The trench DMOS of claim 32, wherein said gate has at least one layer comprising polycide.

40. The trench DMOS of claim 39, wherein said polycide is selected from the group consisting of WSi_2 and $TiSi_2$.

41. The trench DMOS of claim 32, wherein said body region is a P-body.

42. The trench DMOS of claim 32, wherein said body region is disposed on said substrate.

43. The trench DMOS of claim 32, wherein the source region is a source region of said first conductivity type.

44. The trench DMOS of claim 32, further comprising a source region of a third conductivity type.

45. The trench DMOS of claim 44, wherein the first conductivity type is n+ and the third conductivity type is p+.

46. The trench DMOS of claim 32, wherein said source region is an n+ source region.

47. The trench DMOS of claim 32, wherein said source region is adjacent to said trench.

48. The trench DMOS of claim 32, wherein said source region has a junction depth of less than about 0.5 μm.

49. The trench DMOS of claim 32, wherein said source region has a junction depth within the range of about 0.2 to about 0.5 μm.

50. The trench DMOS of claim 32, further comprising a patterned BPSG layer disposed over said trench.

51. A method for forming a trench DMOS transistor cell, comprising the steps of:

providing an article comprising a substrate of a first conductivity type and a body region of a second conductivity type, said article having a trench which extends through said body region and said substrate;

forming a gate overlying said trench and said body region, said gate having at least one layer comprising a material selected from the group consisting of polycide and refractory metals;

placing a mask over the trench;

removing the unmasked portions of the gate; and

forming a first source region in the body region.

52. The method of claim 51, wherein the trench and body region are lined with an insulating layer prior to formation of the gate.

53. The method of claim 51, wherein the first source region is of the first conductivity type.

54. The method of claim 51, wherein the first source region is adjacent to the trench.

55. The method of claim 51, further comprising the step of:

forming a second source region of a third conductivity type.

56. The method of claim 51, wherein the first source region is an n+ source region.

57. The method of claim 55, wherein the first source region is an n+ source region, and wherein the second source region is a p+ source region.

58. The method of claim 51, wherein the step of forming the gate includes the steps of filling the trench with polysilicon, and depositing on the polysilicon a layer comprising a material selected from the group consisting of polycide and refractory metals.

59. The trench DMOS of claim 51 wherein said gate includes at least one layer comprising a material selected from the group consisting of polycide and refractory metals.